Aging Monitoring Methodology for Built-In Self-Test Applications

J. Coelho, J. Semião, C. Leong, M. B. Santos, I. C. Teixeira, J. P. Teixeira

Abstract The high integration level, complexity and performance achieved in new nanometer technologies make IC (Integrated Circuits) products very difficult to test. Moreover, long-term operation brings aging cumulative degradations, and new processes and materials lead to emerging defect phenomena. The consequence is obtaining products with increased variability in their behavior, more susceptible to delay faults and with reduced expected lifecycle. The main purpose of this work is twofold, as explained in the following. First, a new software tool is presented to generate HDL (Hardware Description Language) BIST (Built-In Self-Test) structures, aiming delay faults, and insert the new auto-test functionality in generic sequential CMOS circuits. The BIST methodology used implements a scan based BIST approach, using a new BIST controller to implement the delay-fault techniques Launch-On-Shift (LOS) and Launch-On-Capture (LOC). Second, it will be shown that multi-VDD tests in circuits with BIST infra-structures can be used to detect gross delay faults during on-field operations, and consequently can be used as an aging sensor methodology during circuits' lifecycle. The discrete set of multi-VDD BIST sessions generates a Voltage Signature Collection (VSC), and the presence of a delay-fault (or a physical defect) modifies the VSC collection, allowing the aging sensor capability. The proposed Design for Testability (DFT) method and tool are demonstrated with extensive SPICE simulations using benchmark circuits.

Keywords Built-In-Self-Test, Aging Sensor Methodology, Multi-VDD Tests, HDL automatic generation, Launch-On-Shift, Launch-On-Capture.

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J. Coelho and J. Semião are with Department of Electrical Engineering, ISE - University of Algarve, Faro, Portugal {a16782, jsemiao}@ualg.pt
M. B. Santos, I. C. Teixeira and J. P. Teixeira are with IST, Technical University of Lisbon, Lisboa, Portugal, {marcelino.santos, isabel.teixeira, paulo.teixeira}@ist.utl.pt
C. Leong is with the INESC-ID Lisboa, Lisboa, Portugal, carlos.leong@inesc-id.pt.

1 Introduction

Electronic systems have increased its complexity in the last years in nanotechnologies, which leads to a growth of system functionalities integrated in a single chip. Due to the increased complexity in modern ICs, the impact of testing affects both IC design and manufacturing. It is essential to continuously find/implement new test methods to reduce manufacturing costs and, simultaneously, improve faults' detectability.

Among Design for Testability (DFT) methods, Built-In-Self-Test (BIST) has become a major design consideration and has many advantages. This technique can drastically reduce the external test equipment dependency. Not surprisingly, the International Technology Roadmap for Semiconductors (ITRS), in its 2012 report has placed the design for self-test on the future opportunities in the "Test and Test Equipment" group report [1]. Another important advantage is that BIST allows not only circuit tests during production, but also to test the circuits during their entire lifetime, which is an important feature when long-term degradation effects (aging) start to limit circuits expected life-cycle for nanotechnology ICs. BIST can overcome pin limitations due to packaging, make efficient use of available extra chip area, and provide more detailed information about the faults present. The main disadvantages for BIST usability are, frequently, the

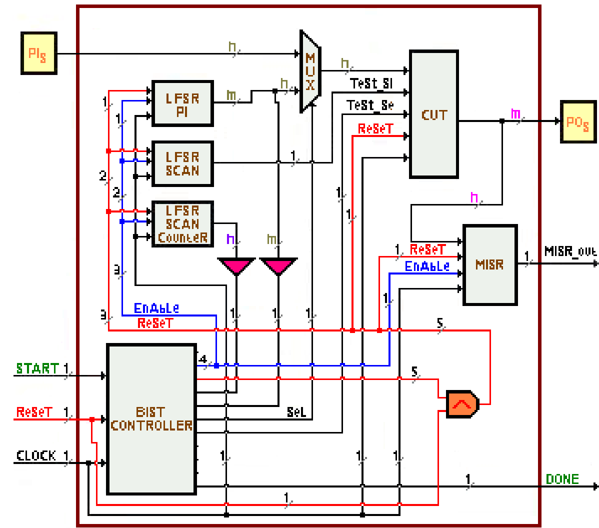
increased die size and design complexity. However, BIST features don't significantly increase today's products size, cost and production time, as was the case in the past.
The purpose of this work is twofold: (1) present a software tool to generate BIST structures automatically and insert them in a circuit under test (CUT), aiming the detection of delay-faults; and (2) show that a set of auto-tests using a variable VDD power-supply voltage source (a set of BIST runs, each run using a different power-supply voltage value) can be used as an aging and performance sensor methodology, for long-term degradations (during circuits' lifespan). In fact, the first purpose is a pre-requisite to the second one.

2. BIST for Delay-faults and Proprietary "BISTGEN" Tool

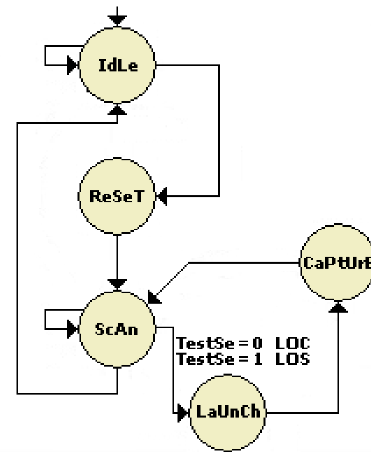
A proprietary BISTGEN tool was developed (using an object-oriented Pascal compiler) to automatically generate and insert BIST structures in a CUT. It's a Windows-based system, and the main purpose is to generate classic scan based BIST structures, merged with delay-fault techniques used in scan: Launch-On-Shift (LOS) and Launch-On-Capture (LOC) [7]. The BIST methodology is defined by the architecture shown in Fig. 1(a). The core unit is the BIST Controller (Fig. 1(b)), which is responsible for controlling how test is applied to the CUT, allowing a LOS strategy, LOC strategy or a combination of both. Starting from an input file containing CUT's description, BISTGEN generates a new VHDL or Verilog type description, containing the CUT and BIST structures.
The original contributions of BISTGEN tool to the scientific community are: (1) the wizard-oriented generation and customization of BIST structures; (2) the generation behavioral or structured BIST descriptions; and (3) a new BIST controller structure and functionality, to allow the use of scan-based delay-fault oriented methods like LOS and LOC.

3. Aging Sensor Methodology

For sequential CUTs, the underlying idea is to reuse on-chip variable power-supply to allow a multi-V_{DD} self-test. Therefore, a discrete set of BIST sessions are performed, for a corresponding discrete set of V_{DD} values, and using the BIST methodology described in previous section. For a given technology, design, temperature and set of BIST sessions, each sample of a fault-free device generates a set



(a)



(b)

Fig. 1 BIST Block: (a) Structure; (b) Controller's state diagram (for LOS or LOC).

of S_i characteristic digital signatures (one for each V_{DD} value), compacted by the MISR as the result of applying n_T test vectors to the CUT, producing the golden VSC (Voltage Signature Collection). In general, VSC is a set of (V_{DDi}, S_i) pairs of values. Temperature variations can shift these digital words along V_{DD} values [2]. Typically, higher temperature shifts the signatures towards lower V_{DD} values [2]. In the presence of aging degradations, some paths will modify their timing response and, as different paths may age differently, the result is a modification in the timing response of the CUT, and the VSC is also modified, allowing the detection of aging degradations in the CUT. This underlying principle of the proposed methodology has been verified by simulation, as will be shown ahead.

4. Simulation Results

This section presents the simulation results for the aging sensor methodology described. Simulations were performed with HSPICE for an ITC'99 benchmark circuit [4], B01 (a Finite State Machine (FSM) that compares serial flow, has 49 logic gates, 2 Primary Inputs (PI), 2 Primary Outputs (PO) and 5 FFs), described in a 65nm PTM technology [6], with a nominal V_{DD} of 1.1V, a -40% VDD variation, and 20 years of aging degradations. Aging degradations were obtained with a proprietary tool *AgingCalc* [3], which uses Vth modulation by calculating signal probabilities to obtain transistors' switching probabilities in a circuit and their aged Vth.

Aging degradation results for B01 circuit are represented in Fig. 2. In this circuit, just for 5 years of lifetime it is possible to spot the two left-most aging variations, signalized in the picture. These are variations in small-delay paths and, therefore, circuit's time-slack is not reduced. For 10 and 15 years of lifetime there are also aging variations detected, but in this picture they can't be spotted. However, a simple inspection on graph's data allows us to detect them. Finally, for 20 years of life-time, a gross-delay variation alters circuit's time-slack (the right-most variation spotted), making the circuit more vulnerable and reducing its reliability.

For bigger circuits, high number of variations in small-delay paths will be spotted, but as mentioned, these do not affect circuit's time slack. On the other hand, the variations spotted in critical paths are the ones that reduce circuit's time-slack and the ones that need user's attention, otherwise circuit may fail. Thus, the margin of V_{DD} values in a VSC collection, for no error spotted, decreases as circuit ages, and this result occurs regardless the circuit's size or complexity.

Moreover, another interesting aspect is that not only CUT's aging degradation can reduce circuit's reliability. BIST circuitry is also subject to aging variations during circuit's lifetime and its CPs may also impose a limit for circuit's performance.

5. Conclusions

In this paper, an aging sensor methodology for BIST circuits was presented, which makes use of circuit's variable power-supply to perform a set of BIST runs at different VDD values and obtain a VSC. This VSC is unique for each sample, and the existence of a delay fault caused by aging degradations during circuit's lifetime

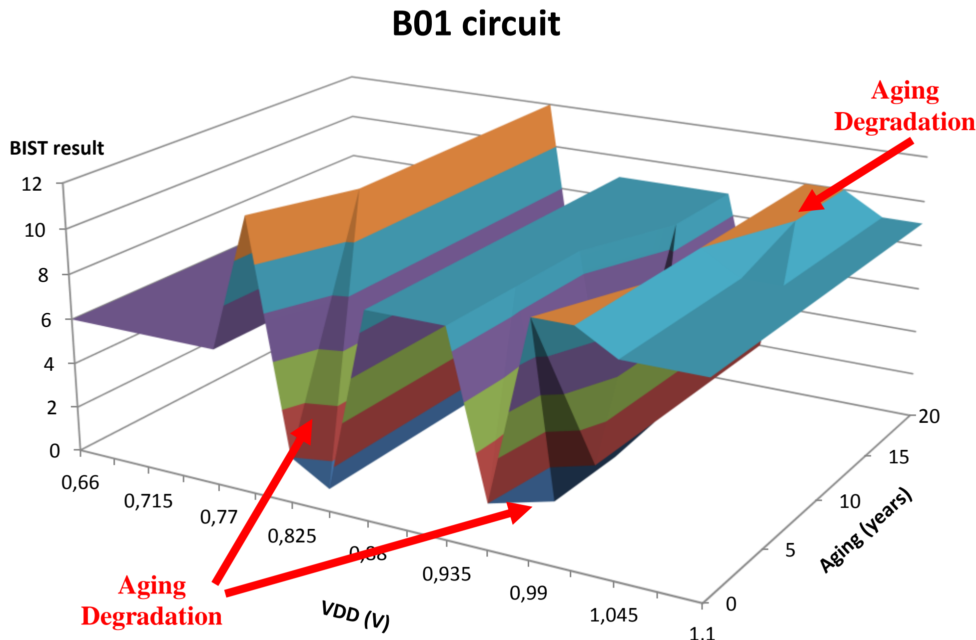


Fig. 2 B01's BIST signatures for VDD and aging variations (VSC evolution with aging).

modifies this VSC, allowing aging monitoring. A proprietary software tool, BISTGEN, was also presented, to automatically generate and insert BIST structures in a CUT, which include LOS and LOC scan strategies, to allow delay-fault detection. The proposed methodology can identify not only gross-delay defects, but also some small delay defects, regardless of their origin.

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