

Automating the Evaluation of Design Choices for Dependable Integrated Circuits

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Abstract—Due to the downscaling of transistor feature sizes, integrated circuits are becoming more susceptible to transient and permanent faults that occur in the field. Systems that are manufactured in those technologies have to be designed fault tolerant in order to still meet certain dependability requirements. This represents a challenging task, as the resulting design space is typically very large and therefore costs and benefits of many different fault tolerance techniques need to be estimated. We propose a tool that supports the design of dependable ICs by automating these estimations for selected design choices. The paper at hand gives an overview on the tool’s intended features and describes how it may be integrated in the design flow.

I. INTRODUCTION

Technology scaling in semiconductor industry causes a higher susceptibility to various fault effects that can lead to transient or permanent faults during the lifetime of integrated circuits (ICs) [1]. ICs that are used in safety-critical applications therefore need to be able to handle these faults in the field. For this reason, many fault tolerance techniques have been developed where each of them affects the system’s dependability individually and causes different costs. These individual costs and benefits have to be estimated during the design phase in order to find a fault tolerant implementation of the circuit that fulfills the respective dependability requirements at acceptable costs. Performing these estimations manually represents a time-consuming and error-prone task, especially if the circuit designer is not an expert in dependability modeling.

Several dependability estimation tools have already been developed decades ago [2]. However, their purpose is only the evaluation of certain dependability models that still need to be constructed by the circuit designer. On the other hand, there are several approaches that introduce some kind of dependability-awareness into an automated design space exploration. Usually they aim at fault tolerance against either permanent faults [3] or transient faults [4]–[6] but not both fault types in combination. Besides that, many of them are based on a library of available processing elements like processors or ASICs whose dependability properties need to be known and are taken as a fact [6]–[8]. Improving these properties, e.g. by applying certain hardware redundancy techniques at RT-level, is not considered in these cases although this could have a significant impact on the result.

This paper presents a tool that is supposed to automate important tasks of the design space exploration for dependable systems without having the aforementioned limitations.

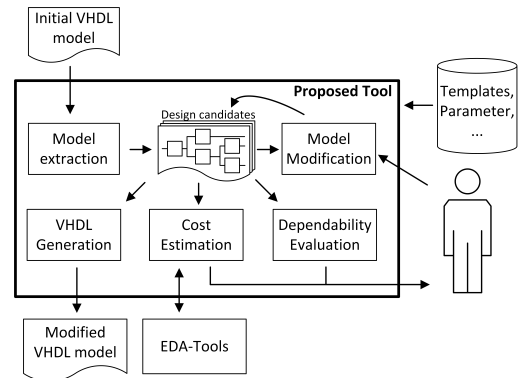


Fig. 1. Steps of the DSE that are automated by the proposed tool

II. THE PROPOSED TOOL

Figure 1 shows how the tool is supposed to be used during the design process. The first step is the analysis of a preliminary VHDL model of the system, whereby the needed information, mainly concerning the system’s structure, is extracted by the tool and stored in a corresponding data structure. This model serves as the starting point for the following design space exploration. Then the circuit designer can choose from a set of fault tolerance techniques that can handle transient and permanent faults by means of hardware redundancy [9]. At selecting the techniques to apply, he has to make several design decisions, e.g. which parts of the system are protected, how many spare components are added, and which online fault handling mechanism is used. The internal model is automatically modified according to these choices, resulting in a set of different design candidates.

In order to determine the most suitable implementation, the individual design candidates have to be evaluated regarding costs and benefits of the applied fault tolerance techniques. These evaluations will be performed automatically by the tool. For this purpose, a few resources like generic VHDL models, script templates for available EDA tools and information on failure rates are provided. Then the cost estimations can be done by generating the corresponding VHDL model of the design candidate and synthesizing it with the help of an external EDA tool. In some cases, rough estimations based on experience values may also be possible. The benefit of the applied fault tolerance methods, i.e. the achieved dependability improvement, is calculated by automatically constructing and solving Markov models.

Based on the results that were obtained during the aforementioned evaluations, the designer can decide which of the implementations meets the actual requirements best or whether another iteration of modifying and evaluating the existing design candidates is necessary. Once the preferred implementation is found, the corresponding VHDL description can be generated by the tool. This allows for an easy integration in established EDA flows.

III. SUMMARY

This paper proposed a new tool for the design of dependable integrated circuits. Its main purpose is the automatic estimation of costs and benefits that are caused by the application of different hardware redundancy based fault tolerance methods. This can significantly accelerate and simplify the design space exploration in order to find an implementation that meets the current dependability requirements at reasonable costs. As the tool takes a VHDL model of the circuit as an input and modifies it according to the selected fault tolerance techniques, the whole approach can easily be integrated in existing EDA flows.

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