Can we trust SET Injection Models?

Varadan Savulimedu Veeravalli, Andreas Steininger
Institute of Computer Engineering
Vienna University of Technology, Vienna (Austria)
Email: {varadan,steininger}@ecs.tuwien.ac.at

Abstract—As the small structures on contemporary ASICs become increasingly sensitive to radiation particle hits, it is important to understand the related effects. Experimental studies referring to this require high efforts, therefore analog-level simulations have become the method of choice. While it is comparatively easy to represent the actual circuit in a simulator like SPICE at any desired level of detail – including parasitic effects, e.g. – the representation of the particle hit is the crucial problem. The state-of-the-art approach is to apply a current pulse with double-exponential shape to a transistor by attaching a current source across its channel terminals. In another, more refined but less popular model two current sources are used, each connected from bulk to one of the channel terminals. In this paper we apply these two different models for the simulation of a Muller C-element and try identify, how much difference the choice of the model for the particle hit actually makes. Our results show that even for this relatively simple target there are already remarkable mismatches in the model predictions, which clearly confirms the need for further research into SET simulation models.

I. INTRODUCTION

In spite of impressive robustness improvements on technology level, the rate of transient errors on modern ASICs caused by radiation particle hits increases. This results from the progressive scaling of the structures and hence critical charges, and the growing number of transistors per chip [1]. It is therefore crucial to devise effective protection mechanisms to keep the error rates of future technology nodes within reasonable bounds. For the design, optimization and validation of such mechanisms the effects of radiation particle hits on a given circuit must be studied. This can either be done in experiments on a physical prototype ASIC [2], which is expensive and inflexible with respect to changes in parameters and circuit, or by means of simulation, where accessibility and flexibility are much better. Not surprisingly, simulation has established itself as the method of choice, more specifically analog-level (SPICE) simulation. As opposed to device-level simulation (like TCAD, e.g.), SPICE simulations remain computationally tractable even for circuits comprising tens of transistors, and still deliver satisfactory accuracy. Pure digital-level simulation, while allowing efficient analysis of even larger circuits, suffers from the too limited means of considering masking effects of the radiation particle hits.

On SPICE level very accurate technology models for the circuit gates, including parasitics, are readily available, and in a post-layout simulation even the interconnect can be well considered. The only problem is the faithful representation of the particle hit. Here, models are available, but these are sub-optimal in some respects. It is the aim of our EASET project\(^1\) to elaborate a better model. To do so, as a first step deficiencies in the state-of-the-art models need to be identified. In this paper we therefore compare the two most advanced models in a concrete study.

As our target cell for this study we chose a Muller C-element, more precisely the implementation by Van Berkel et al. [3]. While this logic element looks simple on the first glance, it provides a number of properties that are useful for our purpose: With its 12 transistors the complexity is easily manageable even for experiments requiring extensive parameter sweeps. Its sequential nature allows us to study whether and how its sensitivity depends on its state. Finally, the Muller C-element is the most fundamental building block in asynchronous (delay-insensitive) design [4].

The paper is structured as follows: In Section II we will survey existing modeling approaches for radiation particle hits in VLSI circuits. Next, Section III will briefly introduce our target cell, namely the Muller C-element. In Section IV we will present setup and results of our experiments and discuss our results in Section V. Finally we will draw the conclusions and give a perspective on future work in Section VI.

II. RELATED WORK

When an energetic particle (charged or uncharged) hits the junction of a transistor, it creates charges that impact the transistor’s operation (this is called a “single-event effect (SEE)”). More specifically, in an open transistor these newly created charges cause an undesired current pulse across the channel [5]. It should be stressed at this point that this is an idealization and in fact part of the charges is also absorbed by the environment. Ultimately, the paths along which the charges actually move depend on many factors, like circuit layout, exact location and energy of particle impact, electromagnetic forces exerted from diverse voltages in the surroundings at the moment of (and right after) the impact, etc. After being converted into voltage through parasitic resistances and capacitances this pulse – then called “single-event transient (SET)” – propagates further, until it is either masked or changes the state of the circuit in an undesired way, which is then termed a “single-event upset (SEU)”.

Clearly, the question whether the SEE will ultimately cause an SEU is fundamental to estimating the soft error rate of a given circuit under given radiation conditions. Therefore SET propagation and masking effects are the most common targets of analog-level simulation studies in this area. Clearly, digital simulation of SEUs, albeit convenient and efficient, does not serve this purpose. It has been found out that the question whether an SET will actually cause an SEU in the end largely depends on the amount of charge it created in the first place.

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For a given circuit node, a “critical charge $Q_{\text{crit}}$” can be determined, above which an SEU will occur. This $Q_{\text{crit}}$ will depend on the circuit state, and so its minimum is normally considered. A number of SPICE analog models have been proposed in literature over the years, which model radiation hits via current injection, and are hence compatible with $Q_{\text{crit}}$ models.

For example, Roche et al. [6] modeled $Q_{\text{crit}}$ as a sum of capacitance and conduction component as shown in eqn. (1).

$$Q_{\text{crit}} = C_N V_{DD} + I_{DP} T_F$$  \hspace{1cm} (1)

In eqn. (1) $C_N$ is the equivalent capacitance of the struck node, $V_{DD}$ the supply voltage, $I_{DP}$ the maximum current of the ON transistor, and $T_F$ the cell flipping time. While capacitance and conductance components do contribute, eqn. (1) overestimates $Q_{\text{crit}}$ because the flipping threshold of an inverter is clearly less than $V_{DD}$. Furthermore $I_{DP}$ considers only the peak value of the current.

The above issues are addressed to some extent by Xu et al. [7] in the following model for an SRAM cell:

$$Q_{\text{crit}} = \int_0^{V_{\text{trip}}} C_N dV + \eta I_P T_{\text{pulse}}$$  \hspace{1cm} (2)

In eqn. (2) $V_{\text{trip}}$ is the static tripping point of the SRAM cell, $I_P$ the driving current of the affected transistor, $T_{\text{pulse}}$ the duration of the particle-induced current pulse, and $\eta$ a correction factor. Even though their $Q_{\text{crit}}$ estimation models the capacitance better, it fails to incorporate the dynamics of voltage transient at the struck node, the quantitative description of $I_P$, and the contributions of different transistors that constitute the cell.

Zhang et al. [8] proposed an analytical technique to estimate $Q_{\text{crit}}$ of an SRAM cell in terms of transistor parameters and the injected current’s amplitude and duration. Unlike the previous ones, their model considers the dynamic response to a particle strike. The only pitfall with this model is that they model the noise source using a rectangular current pulse instead of an exponential one.

Most proposed models agree in the qualitative definition, but differ in essential quantitative aspects [9]. So far the most agreed model to mimic the actual charge deposition mechanism of a particle strike uses double-exponential currents [10], [11], [12], [13].

Wirth et al. [14] proposed an accurate and computer efficient analytical model to evaluate circuit sensitivity. This model predicts whether or not a particle strike generates a pulse that may propagate to the other logic gates or memory elements. They use the double-exponential current model as base for this model. They validated their model using SPICE level simulations in four different technology nodes. In [15] they further calculated the peak voltage and peak time for the double-exponential model to estimate SET propagation in digital circuits. They derive an equation to calibrate the pulse duration for different scenarios and validated their equations using SPICE simulations.

When an $\alpha$-particle or a heavy ion generated by a neutron strike crosses a pn-junction, a funneling process occurs as described by Hseih et al. [16] (charge collection by drift is the dominating phenomenon here). Hellebrand et al. [17] proposed a refined circuit-level model that takes into consideration the charge collected by drift, thereby allowing a variable voltage across the pn-junction. They claim that many SET models do not consider the charge collected by drift and thus do not take into account the varying voltage across the pn-junction. They take the double-exponential model as an example and show that it does not consider varying voltage while generating SETs. They built a current model that calculates the drift current of the particle hit. With the help of the simulations they prove that the refined model reveals twice as many critical effects as the the traditional current model.

Velamala et al. [18] proposed a probability model that examines the propagation of the SET at any node to the output of a circuit. Using the double-exponential model to create the SETs they study how the sensitivity to SETs changes with CMOS technology scaling.

Gili et al. [19] present an SET propagation model that can be used to categorize the propagation likelihood of a given signal. They derive some analytical descriptions for SET pulses in terms of their width and height. The formulas obtained are generic, and they claim that models based on these formulas show a good prediction of pulse propagation. The authors extend this model for being incorporated in CAD tools, to automatically determine the reliability of CMOS ICs against SET effects in [20].

Rohani et al. [21] used the double-exponential model as the base to develop an analytical based pulse determination technique which they validated by pulse determination technique from laser experiments.

Wrobel et al. [22] used an accurate model based on simulation of atmospheric neutron induced transient currents in a 90nm drain electrode, through a detailed diffusion model. They used Monte-Carlo tools to conduct this study. They replaced the transient currents with currents based on double-exponential law. The three parameters of the double-exponential model; rise time, fall time and collected charge are only known approximately. Hence, the authors focused only on the shape of the transient pulse in order to make sure that the double-exponential model is as realistic as possible. Their simulations revealed that the current shape has a small influence on the SEU cross-section and SER. They also prove that they need only two parameters, namely charge collected and the maximum time. The authors conclude that the double-exponential current shape is acceptable to simulate the transient current induced by ionization particles. In [23] they confirm this finding, and they propose to replace the rising time parameter with one fifth of the falling time parameter.

Hamad et al. [24] propose a methodology to abstract model and analyze SET propagation at both transistor and gate level. They model SET at gate level by utilizing transistor level characterization libraries. They identify the vulnerable nodes and inject SETs there, while they also analyze SET propagation for each SET injected. They claim that the new gate-level characterization libraries can accurately analyze SET propagation and estimate the soft error rate at RTL level.
A. Basic Double-Exponential Model used in our experiments

In line with the state of the art we will also use the double-exponential current model for SETs in our experiments. More specifically, for injecting SETs in a transistor of the target circuit we use a current source connected to the source of the transistor that generates a double-exponential current pulse according to eqn. (3) [25]:

\[ I_P(t) = I_0(e^{-t/T\alpha} - e^{-t/T\beta}) \]

Herein, \( I_P \) denotes the transient current pulse, \( I_0 \) the peak current of the two exponential terms, \( T\alpha \) the decay time (fall time) of the current pulse, and \( T\beta \) the time constant for initially establishing the ion track (rise time). Simple calculations reveal that the total charge \( Q_P \) of such a pulse is

\[ Q_P(t) = \int_{0}^{\infty} I_P(t) \, dt = I_0(T\alpha - T\beta), \]

whereas the peak current of the SET (\( I_{peak} \)) is given by

\[ I_{peak} = I_0 \left( e^{\frac{T\beta \log(T\beta/T\alpha)}{T\alpha}} - e^{\frac{T\alpha \log(T\alpha/T\beta)}{T\beta}} \right). \]

Fig. 1: Improved SET Model (a) for PMOS, (b) for NMOS; Double-exponential SET Model (c) for PMOS, (d) for NMOS

The usage of the double-exponential current models on PMOS and NMOS to trigger an SET is presented in Fig. 1(c) and Fig. 1(d). A number of simulations were executed to calibrate the parameters \( I_0 \), \( T\alpha \) and \( T\beta \). By varying all the three parameters to create the same critical charge we observed different shapes of pulses and different pulse widths [26], [27]. In order for our SET model to mimic the particle strike we kept the parameters \( T\beta \) and \( I_0 \) as constant and varied the parameter \( T\alpha \) to vary the critical charge. The parameter \( T\beta \) and \( I_0 \) are set to 10ps and 5mA throughout our simulations.

This single-source double-exponential current model employed in our SPICE model represents the current state-of-the-art which has been considered a suitable trade-off between tractable complexity and sufficient accuracy in most of the related research work. For compatibility with this analysis, and also due to lacking alternatives, we simply had to accept the shortcomings mentioned above. However, our envisioned future work in this area will be devoted to elaborating alternative SPICE models which provide better modeling accuracy with still acceptable complexity.

B. Improved Double-Exponential Model

The SET model proposed by Kleinosowski et al. [28] uses two separate current sources inserted at the source and drain of a transistor to mimic a particle strike. In an NMOS transistor the current flows from the source or drain toward the body as shown in Fig. 1(b). Similarly to mimic a particle strike in the PMOS transistor, the current flows from the body to the source or drain as shown in Fig. 1(a). Having two currents for triggering SET pulses avoids overshoot of voltage above VDD in the device, as seen with the double-exponential current model. We used the parameter setup mentioned for double-exponential current model for triggering SETs using this model.

In our experiments we will apply this model as an alternative to the basic model. This will give us a first indication on where the more detailed modeling of the current flow in the improved model makes a difference.

III. MULLER C-ELEMENT

The Muller C-element (MCE) is a state holding element originally designed by David Muller [29]. With its function representing an AND for transitions, it is the fundamental building block in the design of self-timed circuits. Its output will go high when all its inputs are at high, and the output will go low when all inputs are low. For all other, non-uniform input combinations, the MCE will keep its last valid output level. Note that this property makes the behavior of the MCE not only depend on the inputs but also on its internal state (last valid output) and thus at the input history. Therefore, ultimately, the MCE presents an interesting mix of combinational and sequential behavior, which makes it a perfect (initial) target for our investigations.

In this paper we will consider a 2-input MCE, which is also most often encountered in practice. We denote its inputs 'A' and 'B' and its output 'Z'. Over the years different implementations for the MCE have been proposed [30], of which we chose to use the CMOS Implementation introduced by Van Berkel et al. [3] presented in Fig. 2 as target for our experiments. The output state of the circuit is maintained through a feed-back conducting path of three transistors in the pull-up tree or the pull-down tree. Similar to Sutherland's circuit, this circuit is also ratioless, i.e. its transistor sizes can all be chosen equal.

IV. SET INJECTION EXPERIMENTS

A. Aim of the experiments

Our long term aim is to elaborate a SPICE model for SETs that is accurate enough to allow a faithful simulation of SET propagation and SEU generation in SPICE, i.e. without having to resort to computationally extremely intensive physical level (TCAD) models with their naturally very limited scope. A logical first step towards this end is to investigate the quality of the existing SET models. What we describe here, as a starting point, is to apply the two most advanced models described above in the same way to our target and compare the outcomes. Each mismatch points to a deficiency in one of the models. Without a known-good reference outcome we cannot reliably tell which one is right, and hence we cannot judge the
To get a comprehensive picture, our strategy will be to systematically explore the space spanned by all possible (input and internal) states and all transistors of the MCE. We do, however, not include investigating the MCE’s dynamic behavior here – this has already been done in [31], albeit for the basic double-exponential current model only.

B. Experiment setup

Our target MCE is built in UMC 90nm bulk CMOS technology. We conducted all our simulations using Cadence Spectre and HSPICE simulators. We triggered SETs in all the transistors of the MCE using both SET models. For convenience we name the double-exponential current model “C2” and the improved current model “C1”.

To cover the MCE’s complete possible state space (and different input history) we apply four different input sequences as shown in Table I. Each pattern in the sequence is applied for a duration of $\Delta t$ which is 5ns in our experiment, so one sequence takes 20ns. We repeat the same sequence multiple times to inject SETs in all the transistors, before we change to the next sequence and start over again. The SETs are applied $t_0$ after switching, which is 2ns in our case; so at time 2ns, 7ns, 12ns etc. SETs are injected into a transistor. Note that when we say an SET is “injected into a transistor” this actually means that current is forced on the nodes of the transistor (drain, source, and, in case of the improved model, bulk). With the available models we cannot trigger SETs directly inside the transistor as actual particle hits do.

C. Results

After injecting the SET we observed whether the output of the MCE behaves as in the fault-free case, or it exhibits a deviating behavior. For the latter we could classify our observation into 3 types of behavior:

1) In some cases we observed a transient pulse at Z that, however, did not influence the MCE’s behavior further on, i.e. it did not affect its state. We indicate this case by “SET”.
2) If the injected current was capable of flipping the MCE’s state, i.e. its output Z immediately and had a lasting effect beyond the current pattern, we have experienced an “SEU”.
3) The injected current does not have an immediate effect on the output Z, but when applying the next pattern, the output makes an unexpected, lasting change. We denote this “SEU*”.

Table II summarizes our observations. It can be read as follows: In the first block (lines 3..6) we see the results for injection on transistor $T_0$. The leftmost column specifies the time of injection and thus (by correlation with Table I) to the applied pattern at the time of injection. Column 2 represents the patterns from sequence A and current model C1 (the improved one). The entries “-” indicate that the MCE output behaved exactly as in the fault free case, i.e. the injected fault had no effect. We observe that most of the time the injected SETs had no effect, but for the last pattern in sequence B and the second in sequence D. In those cases we observed an SEU* for with both SET models.

Interestingly, a distinction between inner and outer transistors in the stack becomes apparent: For the outer transistors the models yield the same behavior, but for the inner ones we find two types of discrepancy: (a) $C2$ tends to create SETs at the output that are not seen with C1, in one case ($T_4$, sequence C) we even have an extra SEU. And (b) we observe a kind of time shift in the appearance of some SEU* instances (e.g., $T_3$, sequences B and D).

As an example, let us have a look at figure 3: It illustrates a fault free execution of sequence A in the left part, and then the same execution, but with an SET $C2$ injected at the source terminal of $T_4$ during the input first pattern. With this pattern $T_4$ is open and its source node (bottom trace) floating, as all other transistors connected to that node are open as well. Consequently the injected SET will charge that node positively – while it would normally have stayed at LO, see left part of the trace for comparison. The next pattern then makes $T_5$ conduct, which allows the stored charge to take effect and finally flip the output, causing an SEU. The unexpected thing here is that the SEU is created at a point in time after the SET injection was already finished. This is due to the storing of the charge at the floating node.

Figure 4 illustrates the same experiment for SET model $C1$. As can be seen, the explanation here is not as straightforward, since we inject current in both terminals of $T_4$, which creates a visible effect, namely an SET at the output immediately, but then also flips the state.
TABLE II: Particle Strike Analysis of the C-element

<table>
<thead>
<tr>
<th>Impact Time</th>
<th>Sequence A</th>
<th>Sequence B</th>
<th>Sequence C</th>
<th>Sequence D</th>
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</thead>
<tbody>
<tr>
<td>C1</td>
<td>C2</td>
<td>C1</td>
<td>C2</td>
<td>C1</td>
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<tr>
<td>Particle hit at Transistor T1</td>
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<tr>
<td>T1</td>
<td>T2</td>
<td>T3</td>
<td>T4</td>
<td>T5</td>
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<tr>
<td>Particle hit at Transistor T2</td>
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<td>T6</td>
<td>T7</td>
<td>T8</td>
<td>T9</td>
<td>T10</td>
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<tr>
<td>Particle hit at Transistor T3</td>
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<td>T11</td>
<td>T12</td>
<td>T13</td>
<td>T14</td>
<td>T15</td>
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<td>Particle hit at Transistor T4</td>
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<td>T16</td>
<td>T17</td>
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<td>T20</td>
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<td>Particle hit at Transistor T5</td>
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<td>T21</td>
<td>T22</td>
<td>T23</td>
<td>T24</td>
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<tr>
<td>Particle hit at Transistor T6</td>
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<td>T26</td>
<td>T27</td>
<td>T28</td>
<td>T29</td>
<td>T30</td>
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<tr>
<td>Particle hit at Transistor T7</td>
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<td>T31</td>
<td>T32</td>
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<td>T35</td>
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<td>Particle hit at Transistor T8</td>
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<td></td>
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<td>T36</td>
<td>T37</td>
<td>T38</td>
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<td>T40</td>
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</table>

Fig. 3: Simulation of Van-Berkel C-element with SET at 102ns with Improved SET model

Fig. 4: Simulation of Van-Berkel C-element with SET at 102ns with Double-Exponential SET model

V. DISCUSSION

An analysis of Table II allows us to shed some light on our initial question: Concerning the performance of the SET models we can observe a significant number of differences. Consequently, with respect to our initial question we can state that there is indeed a mismatch between the models, which suggests that at least one of them does not express SET propagation sufficiently accurate. A clear answer on which one is correct (if any) can only be given when using TCAD simulation or physical experiments as a known good reference.

Our preliminary interpretation of these discrepancies is that the limitation of model C2 to inject current just into source or drain terminal is leading to deficiencies, some of which are not seen with model C1 where at least the bulk is available. Since the actual charge flows caused by a particle hit are much more of distributed nature and not at all limited to terminal currents, a further improvement of the model must somehow consider this. However, at the same time analog-level simulators like SPICE are very node-centric and will allow very limited room to move here. Still, our vision is to elaborate a good compromise that provides sufficient accuracy while maintaining the performance benefits of SPICE over physical level simulation.

VI. CONCLUSION

We have performed a comprehensive study of the effects of simulated SETs in a Muller C-element, in which we employed two different models for representing the SET. In one model, the conventional double exponential model, a current source is connected across source and drain terminals of the target transistor, in the other one two current sources are involved, one between source and bulk, and the other between drain and bulk. Our aim was to study whether these models deliver largely comparable predictions or differ in important aspects.

We got some confirmation for this claim from device model simulations and physical micro beam experiments as well, which, however, are out of the scope of this paper.
Our simulation study has identified remarkable discrepancies between the two models. We ascribe this to the different way of modeling charge distribution by those models.

This study was only a very first step towards our aim. Follow-up activities will definitely have to bring insights from physical experiments and from device-level modeling (TCAD) into the picture, where we can accurately trace the flow of charges. By careful analysis of those cases that have turned out problematic in the simulation presented here, we hope to be able to spot the roots of the deviations and get indications on how to improve the model. Our vision is to ultimately have an SET model at hand that can conveniently be used in SPICE, i.e. allowing reasonably sized circuit blocks to be investigated with realistic computational efforts, while providing good accuracy with respect to SET propagation as well as the conversion of SETs into SEUs.

REFERENCES


